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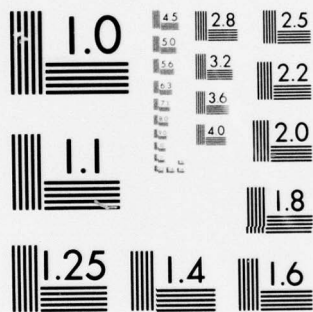
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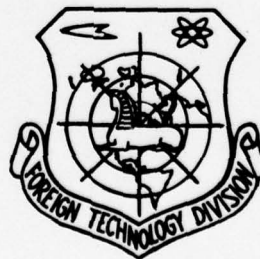
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WITH THE USE OF THE ODRA 1205 COMPUTER

by

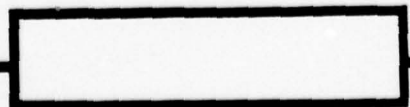
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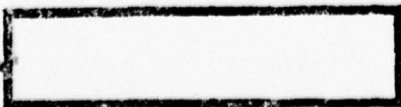
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By: D. Hennig, W. Burkhardt

English pages: 12

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DESIGNING THE TOPOLOGY OF PRINTED CIRCUIT BOARDS with the USE OF THE ODRA
1205 COMPUTER
D. Hennig and W. Burkhardt

1. EXPLANATION OF THE GOAL

In the automatic design process for printed circuits the thought process of the designer has to be abstracted by means of an **appropriate** simulation. Because of the difficulty of reducing creative parts of the **design work** to mathematical formulations and because of the necessity for increasing efficiency through the use of electronic data processing apparatus, simplifications must be made for the functions sought. Initial data for a computer-supported printed circuit board design include:

- circuit diagram,
- circuit part list (standardized description of components),
- data on plug connectors,
- identification and establishment of connection points,
- indication of electrical and thermal restrictions,
- assumption of fixed elements (servo-elements, measuring and testing points, etc.),
- determination of the realizable production class (category),
- data on the **allowance** of a specific number of surfaces (one-sided, two-sided, metallized, multilayer).

The initial data are all in the real area, so that through the placing process and the circuit finding process, both of which are realized in the image area, either a transformation also is necessary or a combination of the two areas must take

place. In the case of the variants presented we made use of the last-mentioned possibility.

2. ORGANIZATIONAL PHASE

Since no simplification such as is possible with the arrangement of identical elements in predetermined places (computer technology or the IC line-up) is possible for the placing of components with very different shapes, one or more target functions must be defined. These target functions are, for example, minimal total conductor length, uniform distribution length, minimal number of required surface changes or avoidance of crossings with limit circuits, consideration of possible spurious couplings of components and conductors, minimum lengths of conductors between specific elements (operating time problems), realization of the circuitry with the least possible waste of technology, etc.

The only limited correlation between target functions does not make it possible to obtain an overall picture of these parameters. In addition, analysis of the minimization of intersections must be dispensed with.

Because of the different criteria laid down for individual circuits we established the simulation principle of placing at a minimum total conductor length as well as the possible con-

sideration of specific restrictions.

The information necessary for placing components, which corresponds to the previously compiled initial data, is put into a form suitable for computer analysis. The circuit diagram is determined with the aid of potential trees (all component terminals which are interconnected correspond to a potential tree) in order to be able to make full utilization of the available computers. This altered form of the simple connection matrix permits a saving of memory space in the case of a coded shutting off of a line or tree. The additional base information consists of a compilation of the dimensions of the components with allowance for their terminals. Here also the projected surfaces lying between the terminals are simplified (or terminals within the projected surfaces are approximated to a rectangle). Finally, the necessary fixed elements and the required assumptions for considering the restrictions are determined.

The placing process is an iterative force simulation principle. The optimal location for each element which is not identified as a fixed element is determined and, if no overlappings with already placed elements appear, the element is placed at this point. According to the simulation principle chosen, that place where the total length of all connections with the element under consideration is minimum is defined as the optimal location.

If there is an overlapping between an already placed element and a new element a meandering investigation of the neighborhood is carried until a free point is found.

In order to prevent a concentration of elements at the plug connector (the fixed element with the most connections) elements which are defined as fixed elements are selected automatically and the distribution of the components on the printed circuit board is homogenized.

The results of the placing phase are the direct input information for the following conductor printing phase. An additional output of the actual component arrangement during the placing process and a graphic representation of the coatings by means of an x-y recorder are provided in order to be able to utilize the available hardware for a control or correction function.

The replacing necessary in the case of the presence of incompatible combinations is performed by determining the coupling capacity appearing between the elements and comparing it with a permissible maximum value.

The coordinates of the terminals of the components with respect to a coordinate system lying with the origin at the mid-point of the board are given as output data.

A transformation of this coordinate system takes place in subsequent realization of the connections.

The information flow of the system is presented in summarized form. (see figure).

3. WIRING PLAN

Computerized designing of the conductor layout on the printed circuit board can begin immediately after the determination of the coordinates of the terminals of the components. Of the initial data on placing the following are used for the wiring plan: connection matrix, coordinates of the component terminals, solder eye diameter, drill hole diameter, and closed areas. The problem of designing the wiring is dealt with after the components are laid out on the printed circuit board. No relocation is performed during the process of laying out the wiring. The rigidly predetermined coordinates of the component terminals must be connected by conductor lines in accordance with the specifications of the connection matrix so that the conductor lines are as short as possible with no crossings.

In addition, the solder eye diameters and drill hole diameters **provided** and the closed areas for the conductor lines (e. g. perforations in the printed circuit board) must be considered in the design.

The number of wiring levels required is a crucial economic criterion for the applicability of a design. Producing the design on one wiring level with the use of the primary and secondary rasters of the circuit board is the goal of the design process proposed. If freedom from crossings in the wiring can not be obtained on one level (e. g. if terminals of the components are surrounded) the appropriate conductor line is broken off and a new conductor line is drawn on the next wiring level required. The number of wiring levels required is kept as low as possible, but may be as many as necessary.

The extent of the preparation of the wiring design requires specification of the method of solution and gradual finishing, since the memory capacity of the ODRA 1204 computer used is only 17 k words (around 11.4 k usable) for every 24 bits in direct access.

The problem segmentation of the of the wiring plan takes place in four phases:

- automatic data preparation of the placing results,
- graph-theoretical optimization,
- a search algorithm for the conductor line plan, and
- automatic correction of the wiring plan.

Because of the small memory capacity of the computer used the individual phases of the plan are treated in different sub-

programs, guaranteeing data matching and no manual preparation of intermediate data being required.

AUTOMATIC DATA PREPARATION OF THE PLACING RESULTS

The placing results are issued on perforated tapes which are used unchanged as input tapes for automatic data preparation. The matching of the transformed coordinates with the nodes of the subgraphs of the connection matrix, the sorting of the subgraphs according to increasing node number, and the determination of the grid coating of the different solder eye diameters are performed in addition to the transformation of the placing coordinates of the pins of the components. The coordinate transformation yields the result that only positive grid coordinates are available for the wiring plan. During the automatic data preparation there are data tests for determining the completeness, freedom from discrepancies, permissible grid coating from solder eyes, and agreement of solder eyes and drill hole diameters. The output data contain the sorted connection trees, the solder eye diameters, and the closed grid coordinates of the circuit board.

OPTIMIZATION ACCORDING TO GRAPH THEORY

The results of the automatic data preparation issued on perforated tapes are used unchanged as input data for optimiza-

tion according to graph theory.

The connection trees under consideration are transformed into minimal structures in accordance with the requirement of the shortest possible conductor lines. The nodes of the subgraphs are permuted in a minimal tree process so that subgraphs with a minimum total of the branch lengths arise. The subgraphs are presented on perforated tapes as a sequence of coordinates to be interconnected, a coordinated potential code number, and the length of the linear continuous branches.

Since freedom from crossings between the minimal trees is not guaranteed the freedom from crossings is checked and the auxillary points for eliminating crossings are determined in the following subprogram. Each branch of a subgraph, beginning with the shortest minimal tree, is developed and recorded as a two-point comparison with its appropriate range of definition. Thus the checking for freedom from crossings may be reduced to a checking of the identity of the direct comparisons of the different branches of different subgraphs. If two direct comparisons in the same range of definition are identical at one point there is a crossing which is eliminated by determining an auxillary point outside of the range of definition of the crossed subgraph. The repeated use of branch division by means of auxillary points and the construction of new subbranches free of crossings is comparable with the threading of connections

between already recorded crossing-free subgraphs.

The sum of the lengths of the connections is indeed raised as compared with the sum of the lengths of the connections of the minimal trees, but the number of the crossings is significantly reduced. If no freedom from crossings is attainable there is a permutation of the nodes within the subgraphs concerned and a repeated checking of the freedom from crossing. If freedom from crossing is not attainable in any case the branch concerned is given according to the original form in the minimal tree.

All branches and subbranches are prepared as input data for the search algorithm on perforated tape with the potential code number and the initial and final coordinates.

SEARCH ALGORITHM FOR THE CONDUCTOR LINE PLAN

The search algorithm in the primary and secondary grids of the circuit board is based on a gradient process with reference to the Lee search algorithm (8 directions in the circuit board grid). Surveying all grid cells according to the classical labyrinth search technique is dispensed with for reasons of memory space and, instead of this, the method of the maximum gradient of the approximation between starting point and goal is used as the dominant criterion. The secondary grid is formed as a function of the primary grid.

All conductor lines can be developed at the same time in step-by-step fashion proceeding from their initial and final coordinates. The grid matrix of the circuit board can be given with a high-speed printer in order to monitor the **current state** during the process of using the search algorithm. The output data on perforated tapes contain the grid covering of the wiring levels of the circuit board and the step-by-step progress of the conductor lines.

AUTOMATIC CORRECTION OF THE WIRING PLAN

After each conductor line is laid out the ~~course of the~~ conductor line is checked and aligned with the aid of a correction program, the task of which is to eliminate all redundant steps in covering the grid with the search algorithm and to make the free grid cells again available to the search algorithm.

Subsequent subprograms make it possible to determine the coupling **capacities** of the conductor line trees and to correct them on the basis of predetermined critical coupling capacities. Parallel parts of conductor lines are partly separated from one another until the critical coupling capacity is no longer exceeded in order to correct the coupling capacity. If this is not possible appropriate information is printed out. No new rerouting takes place.

4. DATA PRODUCTION

The output data of the placing design can be prepared with the aid of a data conversion program so that the production of an automatic drawing of the component coverage of the circuit board is possible. In addition to this there is a transformation of the final data of the placing plan and the wiring plan for the purpose of producing the control data for an automatic drafting machine (ADMAP). The final data are prepared as perforated tapes for drawing the solder eye diagram, for drawing the conductor image, and for drilling the component installation holes. The printed circuit image drawn on glass or film and the drill hole tape are used as data for making master printed circuit boards.

It is necessary to generate all data for the movement of the signal head from the path of the conductor lines in the plan in order to produce the circuit image with the automatic drawing machine. Before a repeated manual aperture change, which in each case takes place in the resting position of the drawing machine, all conductor lines of the same width or solder eyes of the diameter are drawn. High quality drawing machines permit a thorough preparation of the circuit drawing, changing the aperture of the optical head and generating alpha-numerical symbols being performed automatically.

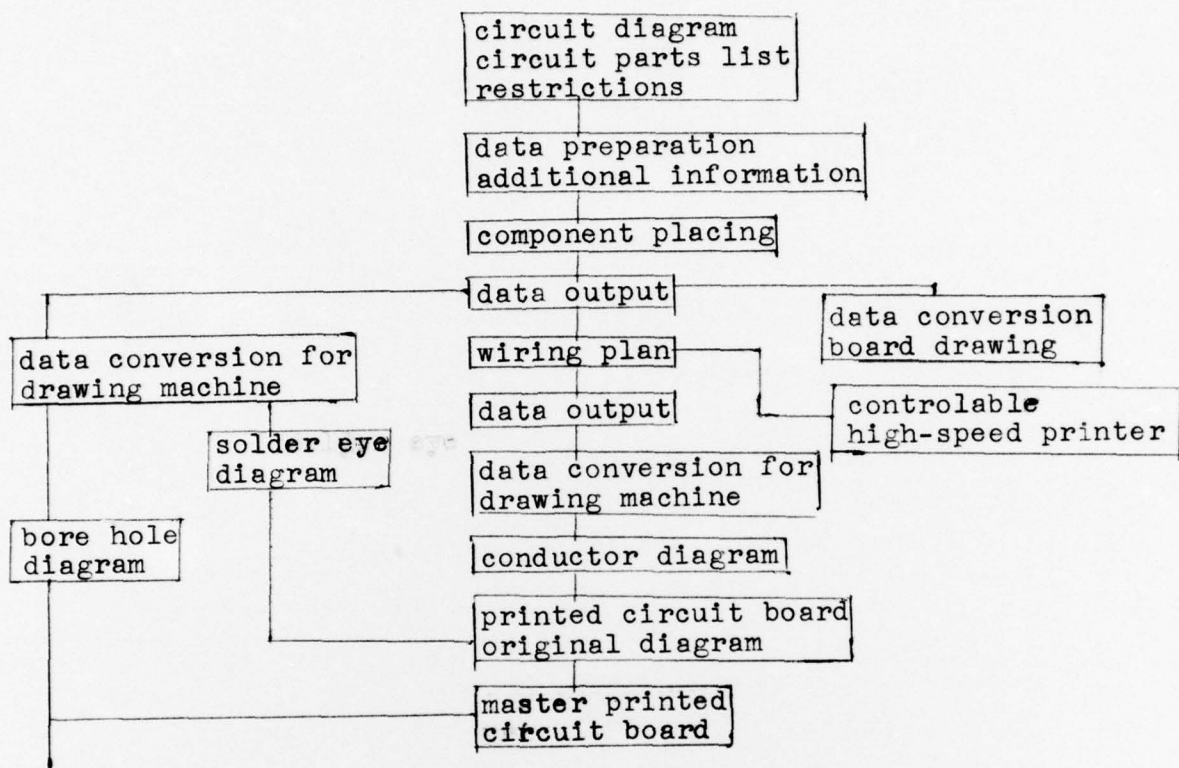


Figure 1. Data flow plan.

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